WHAT IS CLAIMED IS:

1. A ferroelectric memory comprising:

a memory cell which stores data in correspondence with a polarization state of a ferroelectric substance;

a first bit line connected to the memory cell;

a sense amplifier connected to the first bit line;

a first data line to which data is transferred; and

a first column select gate which is formed from a P-channel MOS transistor that has a current path connected between the first bit line and the first data line and is controlled by a column select signal,

wherein while the first data line is set to 0 V, data is read out from the memory cell to the first bit line, amplified and held by the sense amplifier, and transferred from the first bit line to the first data line through the first column select gate by setting the column select signal to low level.

2. The memory according to claim 1, which further comprises a second bit line which is set to a reference potential when the data is read out from the memory cell, and in which the sense amplifier amplifies and holds a potential difference between the first bit line and the second bit line.

3. The memory according to claim 2, wherein the reference potential is an intermediate potential between a potential obtained when "1" data is read out

to the first bit line and that obtained when "0" data is read out to the first bit line.

4. The memory according to claim 2, further comprising a second data line to which data that is complementary to that on the first data line is transferred, and a second column select gate which is formed from a P-channel MOS transistor that has a current path connected between the second bit line and the second data line and is controlled by the column select signal.

5. The memory according to claim 4, further comprising a first N-channel MOS transistor which has a current path connected between the first data line and a ground point and is ON/OFF-controlled by a data line precharge signal, and a second N-channel MOS transistor which has a current path connected between the second data line and the ground point and is ON/OFF-controlled by the data line precharge signal.

6. The memory according to claim 4, further comprising an I/O circuit which is connected to the first and second data lines.

7. The memory according to claim 1, wherein the memory cell comprises one ferroelectric capacitor and one cell transistor.

8. The memory according to claim 7, which further comprises a word line arranged in a direction perpendicular to the first bit line, and a plate line

which is arranged in the direction perpendicular to the first bit line, and

in which one end of a current path of the cell transistor is connected to the first bit line, the other end is connected to one electrode of the ferroelectric capacitor, and a gate of the cell transistor is connected to the word line, and

the other electrode of the ferroelectric capacitor is connected to the plate line.

9. The memory according to claim 2, further comprising a dummy cell which is connected to the second bit line and generates the reference potential.

10. The memory according to claim 9, which further comprises a dummy word line which is arranged in a direction perpendicular to the first bit line, and

in which the dummy cell includes a third N-channel MOS transistor which has a current path with one end connected to the second bit line and the other end connected to a reference voltage source and a gate connected to the dummy word line.

11. The memory according to claim 2, wherein the memory cell comprises first and second ferroelectric capacitors and first and second cell transistors, and the first and second ferroelectric capacitors store complementary data.

12. The memory according to claim 11, which further comprises a word line arranged in a direction

perpendicular to the first and second bit lines, and a plate line which is arranged in the direction perpendicular to the first and second bit lines, and

in which one end of a current path of the first cell transistor is connected to the first bit line, the other end is connected to one electrode of the first ferroelectric capacitor, and a gate of the first cell transistor is connected to the word line,

one end of a current path of the second cell transistor is connected to the second bit line, the other end is connected to one electrode of the second ferroelectric capacitor, and a gate of the second cell transistor is commonly connected to the word line, and

the other electrode of each of the first and second ferroelectric capacitors is commonly connected to the plate line.

13. A ferroelectric memory comprising:

a plurality of memory cell arrays each comprising a plurality of memory cells each of which stores data in correspondence with a polarization state of a ferroelectric substance,

each of the memory cell arrays comprising

a plurality of first bit lines respectively connected to said plurality of memory cells,

a plurality of sense amplifiers respectively connected to said plurality of first bit lines,

a first data line to which data is transferred,

and

a column select circuit which is formed from a plurality of P-channel MOS transistors each of which has a current path connected between the first data line and a corresponding one of said plurality of first bit lines and is controlled by a column select signal,

wherein while the first data line is set to 0 V, data are read out from said plurality of memory cells to said plurality of first bit lines, the column select signal is set to low level and supplied to the gate of each of the plurality of P-channel MOS transistors, and potentials that are amplified and held by said plurality of sense amplifiers are selectively transferred from said plurality of first bit lines to the first data line through the column select circuit.

14. The memory according to claim 13, wherein the column select signal is supplied to the gate of the plurality of P-channel MOS transistors in the column select circuits arranged in the different memory cell arrays.

15. The memory according to claim 13, which further comprises a second bit line which is set to a reference potential when the data is read out from the memory cell, and in which the sense amplifier amplifies and holds a potential difference between the first bit line and the second bit line.

16. The memory according to claim 15, wherein the

reference potential is an intermediate potential between a potential obtained when "1" data is read out to the first bit line and that obtained when "0" data is read out to the first bit line.

17. The memory according to claim 15, further comprising a second data line to which data that is complementary to that on the first data line is transferred, and a second column select gate which is formed from a P-channel MOS transistor that has a current path connected between the second bit line and the second data line and is controlled by the column select signal.

18. The memory according to claim 17, further comprising a first N-channel MOS transistor which has a current path connected between the first data line and a ground point and is ON/OFF-controlled by a data line precharge signal, and a second N-channel MOS transistor which has a current path connected between the second data line and the ground point and is ON/OFF-controlled by the data line precharge signal.

19. The memory according to claim 17, further comprising an I/O circuit which is connected to the first and second data lines.

20. The memory according to claim 13, wherein the memory cell comprises one ferroelectric capacitor and one cell transistor.

21. The memory according to claim 20, which

further comprises a word line arranged in a direction perpendicular to the first bit line, and a plate line which is arranged in the direction perpendicular to the first bit line, and

in which one end of a current path of the cell transistor is connected to the first bit line, the other end is connected to one electrode of the ferroelectric capacitor, and a gate of the cell transistor is connected to the word line, and

the other electrode of the ferroelectric capacitor is connected to the plate line.

22. The memory according to claim 21, further comprising a dummy cell which is connected to the second bit line and generates the reference potential.

23. The memory according to claim 22, which further comprises a dummy word line which is arranged in a direction perpendicular to the first bit line, and

in which the dummy cell includes a third N-channel MOS transistor which has a current path with one end connected to the second bit line and the other end connected to a reference voltage source and a gate connected to the dummy word line.

24. The memory according to claim 15, wherein the memory cell comprises first and second ferroelectric capacitors and first and second cell transistors, and the first and second ferroelectric capacitors store complementary data.

25. The memory according to claim 24, which further comprises a word line arranged in a direction perpendicular to the first and second bit lines, and a plate line which is arranged in the direction perpendicular to the first and second bit lines, and

in which one end of a current path of the first cell transistor is connected to the first bit line, the other end is connected to one electrode of the first ferroelectric capacitor, and a gate of the first cell transistor is connected to the word line,

one end of a current path of the second cell transistor is connected to the second bit line, the other end is connected to one electrode of the second ferroelectric capacitor, and a gate of the second cell transistor is commonly connected to the word line, and

the other electrode of each of the first and second ferroelectric capacitors is commonly connected to the plate line.